L Numb r	Hits	S arch T xt	DB	Tim stamp
1	1	("6100559").PN.	USPAT; US-PGPUB	2002/04/09 10:03
2	1	6100559.URPN.	USPAT	2002/04/09 10:01
3	5	("4889583" | "5674356" | "5679591" | "5918147" | "5933729").PN.	USPAT	2002/04/09 10:02
4	0	257/315.ccls. and @py<2001 and flash and ono and (al2o3 or y203)	USPAT; US-PGPUB	2002/04/09 10:04
5	0	257/315.ccls. and @py<2001 and flash and ono and (al2o3)	USPAT; US-PGPUB	2002/04/09 10:05
6	0	257/315.ccls. and @py<2001 and flash and ono and (alo)	USPAT; US-PGPUB	2002/04/09 10:16
7	0	257/315.ccls. and @py<2001 and flash and ono and aluminum adj oxide	USPAT; US-PGPUB	2002/04/09 10:17
8	1	257/315.ccls. and @py<2001 and flash and aluminum adj oxide	USPAT; US-PGPUB	2002/04/09 10:21
9	1	257/$.ccls. and @py<2001 and flash and dielectric and (y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 10:28
10	2	257/$.ccls. and @py<2001 and flash and dielectric and (al2o3 or y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 10:31
11	0	ono and @py<2001 and flash and dielectric and (al2o3 or y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 10:32
12	0	oxide adj nitride adj oxide and @py<2001 and flash and dielectric and (al2o3 or y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 10:33
13	18	@py<2001 and flash and dielectric and (al2o3 or y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 11:48
14	0	@py<2001 and flash and macronix.as. and (al2o3 or y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 10:35
15	0	macronix.as. and flash and (al2o3 or y2o3 or zrsixoy or hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2o3 or tio2)	USPAT; US-PGPUB	2002/04/09 11:27
16	1	al2o3 and flash and @py<2001 and floating adj gate	USPAT; US-PGPUB	2002/04/09 11:33
17	0	al2o3 and flash and @py<2001 and floating adj gate	JPO	2002/04/09 11:33
18	0	al2o3 and flash and floating adj gate	JPO	2002/04/09 11:33
19	0	257/315.ccls. and (al2o3 or y2o3 r zrsixoy r hfsixoy or la2o3 or zro2 or hfo2 or ta2o5 or pr2 3 r ti 2)	USPAT; US-PGPUB	2002/04/09 11:49
20	0	257/315.ccls. and al2o3	USPAT; US-PGPUB	2002/04/09 11:49

21	0	257/314.ccls. and al2 3	USPAT; US-PGPUB	2002/04/09 12:02
22	22	"5453583"	USPAT; US-PGPUB	2002/04/09 12:02
23	1	("5453583").PN.	USPAT; US-PGPUB	2002/04/09 12:03
24	1	("5729894").PN.	USPAT; US-PGPUB	2002/04/09 12:03
25	1	("5453583").PN.	USPAT; US-PGPUB	2002/04/09 12:04
26	1	("5742477").PN.	USPAT; US-PGPUB	2002/04/09 12:04
27	1	("5801447").PN.	USPAT; US-PGPUB	2002/04/09 12:04
28	1	("5895970").PN.	USPAT; US-PGPUB	2002/04/09 12:05
29	1	("6223429").PN.	USPAT; US-PGPUB	2002/04/09 12:05
30	1	("4983908").PN.	USPAT; US-PGPUB	2002/04/09 12:10
31	1151	365/185.33 and @py<2001	USPAT; US-PGPUB	2002/04/09 12:11
32	1	365/185.33 and @py<2001 and (al2o3 or aluminium adj oxide)	USPAT; US-PGPUB	2002/04/09 14:00
33	1	("5384475").PN.	USPAT; US-PGPUB	2002/04/09 14:01
34	1	("6117792").PN.	USPAT; US-PGPUB	2002/04/09 14:01
35	1	("5801447").PN.	USPAT; US-PGPUB	2002/04/09 14:01
36	1	("6087201").PN.	USPAT; US-PGPUB	2002/04/09 14:02
37	1	("6133069").PN.	USPAT; US-PGPUB	2002/04/09 14:15
38	1	("5644533").PN.	USPAT; US-PGPUB	2002/04/09 14:16
39	5	5644533.URPN.	USPAT	2002/04/09 14:16
40	1941	aluminum adj oxide and flash and @py<2001	USPAT; US-PGPUB	2002/04/09 14:17
41	265331	aluminum adj oxide and flash and floating gate and @py<2001	USPAT; US-PGPUB	2002/04/09 14:18
42	21	aluminum adj oxide and flash and floating adj gate and @py<2001	USPAT; US-PGPUB	2002/04/09 14:19
43	8	aluminum adj oxide same dielectric and flash and floating adj gate and @py<2001	USPAT; US-PGPUB	2002/04/09 15:19
44	1853	257/314-326.ccls. and @py<2001	USPAT; US-PGPUB	2002/04/09 15:20
45	72	257/314-326.ccls. and @py<2001 and aluminum adj xid	USPAT; US-PGPUB	2002/04/09 15:21
46	12	257/314-326. cls. and @py<2001 and aluminum adj xide and flash	USPAT; US-PGPUB	2002/04/09 15:22
47	0	257/295.ccls. and @py<2001 and aluminum adj xid and flash	USPAT; US-PGPUB	2002/04/09 15:22

48	356	257/295.ccls. and @py<2001	USPAT; US-PGPUB	2002/04/09 15:22
49	47	257/295.ccls. and @py<2001 and flash	USPAT; US-PGPUB	2002/04/09 15:22
-	167	257/781.ccls. and @py<2001	USPAT	2002/03/26 11:47

FILE 'REGISTRY' ENTERED AT 10:07:12 ON 09 APR 2002

L1 8 S "AL2 O3"/MF

FILE 'HCAPLUS' ENTERED AT 10:11:32 ON 09 APR 2002

L2 2313 S L1(L)DIELECTRIC
L3 1 S L2 AND FLASH MEMORY
L4 38 S L2 AND TUNNEL######
L5 4 S L2 AND FLOATING GATE
L6 51 S L2 AND MEMORY
L7 2 S L2 AND CONTROL GATE
L8 12 S L2 AND SOURCE(2A)DRAIN
L9 548 S L2 AND SUBSTRATE
L10 46 S L2 AND STACK####
L11 83536 S DIELECTRIC CONSTANT
L12 52138 S ("DIELECTRIC CONSTANT"/CT OR . . . .)
L13 493 S L2 AND L12
L14 520 S DIELECTRIC(2A)STACK#####
L15 38 S L1 AND L14
L16 752 S L2 AND L11
L17 847 S L13 OR L16
L18 14 S L17 AND L4
L19 9 S L17 AND L6
L20 150 S L17 AND L9
L21 13 S L17 AND L10
L22 145 S L2 AND L9 AND L11
L23 2 S L4 AND L6 AND L9
L24 1 S L4 AND L6 AND L10
L25 1 S L4 AND L6 AND L11
L26 0 S L4 AND L6 AND L12
L27 0 S L4 AND L6 AND L13
L28 1 S L4 AND L6 AND L14
L29 1 S L4 AND L6 AND L17
L30 1 S L4 AND L6 AND L20
L31 3 S L22 AND L4
L32 3 S L22 AND L6
L33 7 S L22 AND L10
L34 1 S L22 AND L14
L35 7 S L4 AND L6
L36 7 S L4 AND L9
L37 5 S L4 AND L10
L38 4 S L4 AND L14
L39 89124 S (L11 OR L12)
L40 14 S L4 AND L39
L41 20 S L6 AND L9
L42 4 S L6 AND L10
L43 1 S L6 AND L14
L44 3 S L6 AND L20
L45 3 S L6 AND L22
L46 23 S L9 AND L10
L47 20 S (L4 OR L6 OR L10) AND VOLTAGE
L48 1527 S TUNNELING EFFECT OR TUNNELLING EFFECT
L49 0 S (L4 OR L6 OR L10) AND L48
L50 22 S CHANNEL HOT ELECTRON INJECT####
L51 373 S HOT ELECTRON INJECT####
L52 526 S HOT ELECTRON(2A)INJECT####
L53 1834 S FOWLER NORDHEIM
L54 52 S "F" "N" TUNNEL#####
L55 133 S (WRITE OR WROTE OR WRITTEN OR ERAS#####) AND (L48 OR (L50 OR L51 OR L52 OR L53 OR L54))
L56 0 S L55 AND L1
L57 24 S L55 AND DIELECTRIC
L58 54 S L55 AND FLASH
L59 1469 S CONTROL GATE
L60 2283 S FLOATING GATE

FILE 'HCAPLUS' ENTERED AT 10:11:32 ON 09 APR 2002

```
L61     30 S  L58 AND (L59 OR L60)
L62   1096 S  L59 AND L60
L63      6 S  L61 AND DIELECTRIC
L64      2 S  L2 AND L62
L65      9 S  L1 AND L62
L66      2 S  L62 AND DIELECTRIC STACK#####
L67    192 S  L3 OR L5 OR (L7 OR L8) OR (L18 OR L19) OR L21 OR (L23 OR L24 OR L25 OR L26 OR L27 OR L28
              OR L29 OR L30 OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38) OR (L40 OR L41
              OR L42 OR L43 OR L44 OR L45 OR L46 OR L47) OR L50 OR (L57 OR L58) OR L61 OR (L63 OR L64
              OR L65 OR L66)
L68     97 S  L18 OR L40 OR L3 OR L5 OR (L7 OR L8) OR L19 OR L21 OR (L23 OR L24 OR L25 OR L26 OR L27
              OR L28 OR L29 OR L30 OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38) OR (L41
              OR L42 OR L43 OR L44 OR L45) OR L47 OR (L63 OR L64 OR L65 OR L66)
L69     56 S  L67 AND TUNNEL###### AND GATE
       SEL RN
L70     63 S  L67 AND FLASH
L71     81 S  (L69 OR L70)
L72     29 S  L71 AND DIELECTRIC
       SEL RN
L73     23 S  L72 AND (7440-21-3/BI OR 7631-86-9/BI OR 12033-89-5/BI OR 1344-28-1/BI OR . . . . )
L74      6 S  L72 NOT L73
L75      8 S  L50 AND FLASH
L76      8 S  L75 NOT L72
       SEL RN
L77      2 S  L76 AND (7440-21-3/BI OR 12033-89-5/BI OR 7631-86-9/BI OR 7664-41-7/BI)
L78      6 S  L76 NOT L77
L79     12 S  ((L2 OR L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10) OR L14) AND (L51 OR L52 OR L53 OR
              L54 OR L55)
L80     26 S ((L2 OR L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10) OR L14 OR (L51 OR L52 OR L53 OR L54 OR
              L55)) AND (MINIMI####### OR MINIMUM OR LESS#### OR REDUC#####)(2A)(VOLTAGE OR POTENTIAL)
L81    271 S  ((L2 OR L3 OR L4 OR L5 OR L6 OR L7 OR L8 OR L9 OR L10) OR L14 OR (L51 OR L52 OR L53 OR
              L54 OR L55)) AND CURRENT(2A)(LEAK#### OR LOSE OR LOST OR LOSING)
L82    129 S  L81 AND (VOLTAGE OR POTENTIAL)
L83     74 S  L82 AND DIELECTRIC
L84     28 S  L83 AND (STACK##### OR MULTILAYER##### OR MULTI OR MULTIPLE OR (TRI OR TRIPLE OR
              TRIPLY OR TERNARY OR THREE)(W)(FILM OR LAYER####))
L85     62 S  ((L79 OR L80) OR L84) NOT (L72 OR L76)
L86      9 S  L85 AND MEMORY
L87      4 S  L85 AND FLASH
L88      9 S  (L86 OR L87)
       SEL RN
L89      7 S  L88 AND (7631-86-9/BI OR 7440-21-3/BI OR 12033-89-5/BI OR 10024-97-2/BI OR 10102-43-9/BI OR
              11105-01-4/BI OR 15888-69-4/BI OR 7723-14-0/BI)
L90      2 S  L88 NOT L89
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FILE 'REGISTRY' ENTERED AT 10:49:18 ON 09 APR 2002

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L91     56 S  (N4 SI3 OR O3 Y2 OR HF O2 OR O2 SI)/MF
L92     79 S  O SI ZR/ELF
L93      4 S  LA2 O3/MF
L94     14 S  O2 ZR/MF
L95      8 S  HF O SI/ELF
L96      3 S  O5 TA2/MF
L97      1 S  O3 PR2/MF
L98     87 S  O PR/ELF
L99     10 S  "HF O PR"/ELF OR ("HF O PR Y"/ELF OR "HF O PR Y ZR"/ELF)

L100  2412 S  (FLASH OR MEMORY) AND DIELECTRIC AND
              (L91 OR L92 OR L93 OR L94 OR L95 OR L96 OR L97 OR L98 OR L99)
L101    23 S  L95 OR L99
       SEL RN
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FILE 'HCAPLUS' ENTERED AT 10:52:34 ON 09 APR 2002

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L102     23 S L101 AND (12423-21-1/BI OR 12055-23-1/BI OR . . . . )
L103    367 S L100 AND FLOATING GATE
L104    229 S L103 AND CONTROL GATE
L105    105 S L104 AND (TUNNEL###### OR (L50 OR L51 OR L52 OR L53 OR L54 OR L55))
L106     60 S L105 AND SOURCE AND DRAIN
L107     22 S L106 AND STACK######
L108      3 S L106 AND (PROGRAM##### OR APPLIED OR APPLY###### OR APPLICATION OR
                APPLIES)(3A)(VOLTAGE OR POTENTIAL)
L109     88 S L3 OR L5 OR (L7 OR L8) OR L19 OR (L23 OR L24 OR L25 OR L26 OR L27 OR L28 OR L29 OR L30
              OR L31 OR L32 OR L33 OR L34 OR L35 OR L36 OR L37 OR L38) OR (L42 OR L43 OR L44 OR L45)
              OR (L63 OR L64 OR L65 OR L66) OR (L74 OR L75 OR L76 OR L77 OR L78 OR L79) OR (L86 OR L87
              OR L88 OR L89 OR L90)
L110     62 S L72 OR L76 OR L102 OR L90
L111     25 S (L107 OR L108) NOT L110
            SEL RN
L112     25 S L111 AND (7631-86-9/BI OR 7440-21-3/BI OR 12033-89-5/BI OR 7723-14-0/BI OR . . . . )
L113     62 S L109 NOT (L110 OR L111)
L114      0 S L113 AND FOUR STATE
L115      1 S FOUR STATE AND FLASH
L116      7 S FOUR STATE AND MEMORY
L117  39239 S (SINGLE OR ONE)(2A)CELL
L118    934 S (SINGLE OR ONE)(2A)MEMORY
L119     76 S TWO BIT
L120     58 S L113 AND DIELECTRIC
L121      2 S L113 AND (BANDGAP OR BAND GAP OR ENERGY GAP OR WIDEBAND OR WIDE BAND OR WIDE
                GAP OR WIDEGAP)
L122      3 S L113 AND STACK#####/TI AND (FLASH OR MEMORY)/TI
L123      4 S L113 AND TUNNEL######/TI AND STACK######
L124      0 S L113 AND (L117 OR L118 OR L119)
L125     88 S (FLASH OR MEMORY) AND DIELECTRIC AND (L117 OR L118 OR L119)
L126      8 S L125 AND STACK######
L127     25 S (L115 OR L116) OR (L121 OR L122 OR L123) OR L126
L128     25 S L127 NOT (L110 OR L111)
            SEL RN
L129     22 S L128 AND (12033-89-5/BI OR 7440-21-3/BI OR . . . . )
L130      3 S L128 NOT L129
L131  15961 S HIGH(W)("K" OR KAPPA OR DIELECTRIC OR DIELEC)
L132    153 S L131 AND (OXIDE OR INSULAT###### OR DIELECTRIC OR DIELEC)(1A)(STACK###### OR
                MULTI OR MULTIPLE OR MULTILAYER#####)
L133     13 S L132 AND (FLASH OR MEMORY)/TI,ST,IT
L134     13 S L133 NOT (127 OR L110 OR L111)
            SEL RN
L135     11 S L134 AND (12033-89-5/BI OR 7440-21-3/BI OR . . . . )
L136      2 S L134 NOT L135
L137      3 S FLASH MEMORY AND (TWO OR SECOND)(W)OXIDE(W)
              (LAYER##### OR FILM OR STACK#### OR MULTILAYER#####)
            SEL RN
L138      3 S L137 AND (12033-89-5/BI OR 7440-21-3/BI OR . . . . )
L139     31 S FLASH MEMORY AND SOURCE(8A)SUBSTRATE AND
              DRAIN(8A)SUBSTRATE AND (FLOAT### OR GATE)(8A)SUBSTRATE
L140    121 S L129 OR L135 OR L138 OR (L110 OR L111)
L141     28 S L139 NOT L140
L142      0 S (L48 OR (L50 OR L51 OR L52 OR L53 OR L54)) AND L141
L143     14 S DIELEC AND L141
            SEL RN
L144     14 S L143 AND (12033-89-5/BI OR 7440-21-3/BI OR . . . . )
L145      8 S FLASH MEMORY AND SOURCE(4A)SUBSTRATE AND
            DRAIN(4A)SUBSTRATE AND (FLOAT### OR GATE)(4A)SUBSTRATE
L146      4 S L145 NOT L144
            SEL RN
L147      4 S L146 AND (7440-21-3/BI OR 12033-89-5/BI OR 7631-86-9/BI OR 7440-38-2/BI OR . . . . )
```

L135 ANSWER 7 OF 11 HCAPLUS

AN 2000:238023 HCAPLUS
DN 132:245023
TI **Flash memory** device having high permittivity **stacked dielectric** and fabrication thereof
IN Gardner, Mark I.; Gilmer, Mark C.; Spikes, Thomas E., Jr.
PA Advanced Micro Devices, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
IC ICM H01L021-336
NCL 438257000
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6048766	A	20000411	US 1998-172410	19981014

AB A memory device having a high performance **stacked dielec**. sandwiched between two polysilicon plates and method of fabrication thereof is provided. A memory device, in accordance with an embodiment, includes two polysilicon plates and a high permittivity **dielec. stack** disposed between the two polysilicon plates. The high permittivity **dielec. stack** includes a relatively high permittivity layer and two relatively low permittivity buffer layers. Each buffer layer is disposed between the relatively high permittivity layer and a resp. one of the two polysilicon plates. The high permittivity layer may, for example, be a barium strontium titanate and the buffer layers may each include a layer of silicon nitride adjacent the resp. polysilicon plate and a layer of titanium dioxide between the silicon nitride and the barium strontium titanate. The new high performance dielec. layer can, e.g., increase the speed and reliability of the memory device as compared to conventional memory devices.

ST **flash memory** device **stacked dielec** fabrication; permittivity **high dielec flash memory** device

IT Dielectric constant
Dielectric films
Electric insulators
Semiconductor device fabrication
(**flash memory** device having high permittivity **stacked dielec**. and fabrication thereof)

IT **Memory** devices
(**flash; flash memory** device having high permittivity **stacked dielec**. and fabrication thereof)

IT Vapor deposition process
(plasma; **flash memory** device having high permittivity **stacked dielec**. and fabrication thereof)

IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses **13463-67-7**, Titania, uses **37305-87-6**, Barium strontium titanate
RL: DEV (Device component use); USES (Uses)
(**flash memory** device having high permittivity **stacked dielec**. and fabrication thereof)

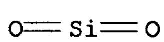
L135 ANSWER 5 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:467884 HCAPLUS
DN 133:67369
TI **Stacked** tunneling **dielectric** technology for improving data retention of EEPROM cell
IN Li, Xiao-Yu; Xiang, Qi; Mehta, Sunil D.
PA Lattice Semiconductor Corp., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6087696	A	20000711	US 1998-86437	19980528

AB An improved EEPROM cell structure and a method of fabricating the same is provided so as to improve data retention. The EEPROM cell includes a **stacked dielec.** structure consisting of a thin tunnel oxide layer and a **high-k** dielec. layer to function as the tunneling dielec. barrier so as to suppress leakage current.
IT **1314-61-0**, Tantalum pentoxide **1344-28-1**, Alumina, processes **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabrication of **stacked** tunneling **dielec.** technol. for improving data retention of EEPROM cell)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 1344-28-1 HCAPLUS
CN Aluminum oxide (Al2O3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7440-21-3**, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(poly; in fabrication of **stacked** tunneling **dielec.** technol. for improving data retention of EEPROM cell)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L90 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 1995:580688 HCAPLUS
DN 122:328454
TI Nonvolatile electrically **erasable memory** device and its manufacture
IN Walker, Andrew Jan; Cuppens, Roger; Kronert, Alwin Nils
PA Philips Electronics N.V., Neth.
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM H01L029-788
ICS H01L027-115
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 642172	A1	19950308	EP 1994-202482	19940831
	EP 642172	B1	19981104		
	R: DE, FR, GB, IT, NL				
	BE 1007475	A3	19950711	BE 1993-912	19930906
	JP 07094613	A2	19950407	JP 1994-211187	19940905
	US 5895950	A	19990420	US 1997-838247	19970417
PRAI	BE 1993-912		19930906		
	US 1994-301443		19940906		

AB The invention relates to a nonvolatile **memory** with floating gate, in particular a **flash** EPROM, in which writing takes place through **injection** of **hot electrons** into the floating gate and in which **erasing** takes place through injection of hot holes. To keep the **write** and **erase** voltages sufficiently low, p-type zones which locally increase the background doping concn. of the p-type substrate are provided around the n-type source and drain zones. These p-types zones cause an increase field strength at the drain zone whereby hot electrons are formed at the pinch-off point also at lower voltages. This increased background concn. in addn. **reduces** the breakdown **voltage** of the p-n junction of the source and drain zones, so that hot holes for **erasing** can be formed by p-n breakdown even at comparatively low voltages. The device is particularly suitable for being integrated into a signal-processing integrated circuit manufd. in a std. process, such as a microcontroller.
ST nonvolatile elec **erasable memory** device manuf
IT **Memory** devices
(read-only, **erasable** programmable, **flash**; having low **write** and **erase** voltages)

L129 ANSWER 12 OF 22 HCAPLUS
AN 2000:568495 HCAPLUS
DN 133:143619
TI Dielectric layer of **memory** cell having **stacked** oxide sidewall and fabrication of same
IN Deustcher, Neil; Wong, Jack
PA Microchip Technology Incorporated, USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6103576	A	20000815	US 1999-290271	19990413

AB A merged two-transistor memory cell of an EEPROM, and method for fabrication of the cell are provided. The memory cell includes a substrate and gate oxide layer formed on the substrate. It also includes a memory transistor having a **floating gate** and a **control gate**, and a select transistor having a gate that is shared with the memory transistor. The memory cell is configured so that the shared gate serves both as the **control gate** of the memory transistor and the wordline of the select transistor. The memory cell further includes a dielec. layer that is disposed between the **floating gate** and the shared gate. The dielec. layer is defined by an oxide/nitride/oxide (ONO) stack film and a stacked oxide layer. In fabricating the memory cell, the ONO stack film is formed adjacent to the top surface of the **floating gate** and the stacked oxide layer is formed adjacent to the side surface of the **floating gate**.

IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses **12039-88-2**, Tungsten silicide **12627-41-7**, Tungsten silicide
RL: DEV (Device component use); USES (Uses)
(dielec. layer of memory cell having stacked oxide sidewall and fabrication of same)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si_3N_4) (8CI, 9CI) (CA INDEX NAME)

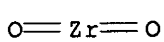
L129 ANSWER 2 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:595418 HCAPLUS
DN 135:161210
TI Multilayer **dielectric stack** with thin high constant materials and low **tunneling** current and method of depositing
IN Ma, Yanjun; Ono, Yoshi
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1124262	A2	20010816	EP 2001-301136	20010208
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2001267566	A2	20010928	JP 2001-20773	20010129
PRAI	US 2000-502420	A	20000211		

AB A multilayer **dielec. stack** is provided which has alternating layers of a high-k material and an interposing material. The presence of the interposing material and the thinness of the high-k material layers reduces or eliminate effects of crystn. within the high-k material, even at relatively high annealing temps. The high-k dielec. layers are a metal oxide of preferably Zr or Hf. The interposing layers are preferably amorphous Al oxide, Al nitride, or Si nitride. Because the layers reduce the effects of cryst. structures within individual layers, the overall **tunneling** current is reduced. Also provided are at. layer deposition, sputtering, and evapn. as methods of depositing desired materials for forming the above-mentioned multilayer **dielec. stack**.

IT **1314-23-4P**, Zirconium dioxide, processes **1314-61-0P**, Tantalum pentoxide **1344-28-1P**, Aluminum oxide, processes **7631-86-9P**, Silica, processes **11105-01-4P**, Silicon nitride oxide **12033-89-5P**, Silicon nitride, processes **12055-23-1P**, Hafnium dioxide **13463-67-7P**, Titania, processes **24304-00-5P**, Aluminum nitride
RL: PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
(multilayer **dielec. stack** with thin high const. materials and low **tunneling** current and method of depositing)

RN 1314-23-4 HCAPLUS
CN Zirconium oxide (ZrO2) (8CI, 9CI) (CA INDEX NAME)



RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 1344-28-1 HCAPLUS
CN Aluminum oxide (Al2O3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 11105-01-4 HCAPLUS
CN Silicon nitride oxide (9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 12055-23-1 HCAPLUS
CN Hafnium oxide (HfO2) (8CI, 9CI) (CA INDEX NAME)

O=Hf=O

RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)

O=Ti=O

RN 24304-00-5 HCAPLUS
CN Aluminum nitride (AlN) (9CI) (CA INDEX NAME)

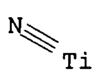
N≡Al

IT **12033-89-5P**, Silicon mononitride, processes
RL: PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); PROC (Process); USES (Uses)
(solid; multilayer **dielec. stack** with thin high const. materials and low **tunneling** current and method of depositing)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L135 ANSWER 6 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:277523 HCAPLUS
DN 132:302092
TI DRAM **memory** cell stacked capacitors having **high dielectric multilayer** films and fabrication thereof
IN Shin, Dong Won
PA Samsung Electronics Co., Ltd., S. Korea
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

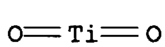
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000124425	A2	20000428	JP 1999-89896	19990330
	US 6300215	B1	20011009	US 1999-417859	19991014
	US 2001042878	A1	20011122	US 2001-903153	20010711
PRAI	KR 1998-43554	A	19981019		
	US 1999-417859	A3	19991014		

AB The title fabrication of stacked charge-storage cell capacitors involves depositing a polysilicon node on a gate which is formed on a semiconductor substrate, depositing Ti on the polysilicon node, annealing the deposited Ti in N2 atm. to give a Ti nitride film, depositing a Ta2O5 on the Ti nitride film, annealing the in O2 atm. at 700-900.degree. to give Ti oxide, and subsequently providing a plate electrode. The process provides TiO2/Ta2O5 or SiON/TiO2/Ta2O5 composite dielec. film with significantly decreased current leakage and increased cell capacitance.
IT **25583-20-4,** Titanium nitride (TiN)
RL: RCT (Reactant)
(DRAM **memory** cell stacked capacitors having **high dielec. multilayer** films and fabrication thereof)
RN 25583-20-4 HCAPLUS
CN Titanium nitride (TiN) (7CI, 8CI, 9CI) (CA INDEX NAME)



IT **1314-61-0P,** Tantalum oxide (Ta2O5) **13463-67-7P,** Titanium oxide (TiO2), properties
RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(TiO2/Ta2O5 composite dielec. films; DRAM **memory** cell stacked capacitors having **high dielec. multilayer** films and fabrication thereof)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)



L135 ANSWER 7 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:238023 HCAPLUS
DN 132:245023
TI **Flash memory** device having high permittivity **stacked dielectric** and fabrication thereof
IN Gardner, Mark I.; Gilmer, Mark C.; Spikes, Thomas E., Jr.
PA Advanced Micro Devices, USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6048766	A	20000411	US 1998-172410	19981014

AB A memory device having a high performance **stacked dielec**. sandwiched between two polysilicon plates and method of fabrication thereof is provided. A memory device, in accordance with an embodiment, includes two polysilicon plates and a high permittivity **dielec. stack** disposed between the two polysilicon plates. The high permittivity **dielec. stack** includes a relatively high permittivity layer and two relatively low permittivity buffer layers. Each buffer layer is disposed between the relatively high permittivity layer and a resp. one of the two polysilicon plates. The high permittivity layer may, for example, be a barium strontium titanate and the buffer layers may each include a layer of silicon nitride adjacent the resp. polysilicon plate and a layer of titanium dioxide between the silicon nitride and the barium strontium titanate. The new high performance dielec. layer can, e.g., increase the speed and reliability of the memory device as compared to conventional memory devices.
IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses **13463-67-7**, Titania, uses **37305-87-6**, Barium strontium titanate
RL: DEV (Device component use); USES (Uses)
(**flash memory** device having high permittivity **stacked dielec.** and fabrication thereof)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)

L135 ANSWER 8 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:212127 HCAPLUS
DN 128:237598
TI Stacked type DRAM cell technology in gigabit era
AU Oji, Yuzuru
CS Dep. Semicond. Bus., Hitachi Ltd., Japan
SO Handotai Kenkyu (1997), 43(Cho LSI Gijutsu, 21), 59-83
CODEN: HAKEFA
PB Kogyo Chosakai
DT Journal; General Review
LA Japanese
AB A review with 50 refs., on the current trend for stacked cell technol., capacitor structures, and **high-dielec**. insulator films such as Ta2O5, BST, and PZT films.
IT **1314-61-0P**, Tantalum oxide (Ta2O5) **7631-86-9P**, Silica, properties **12033-89-5P**, Silicon nitride, properties **12626-81-2P**, Lead titanate zirconate **37305-87-6P**, Barium strontium titanate
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); PROC (Process); USES (Uses)
(**dielec**. film; **stacked** type DRAM cell technol. in gigabit era)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 12626-81-2 HCAPLUS
CN Lead titanium zirconium oxide (Pb(Ti,Zr)O3) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	3	17778-80-2
Zr	0 - 1	7440-67-7
Ti	0 - 1	7440-32-6
Pb	1	7439-92-1

RN 37305-87-6 HCAPLUS
CN Barium strontium titanium oxide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	x	17778-80-2
Ba	x	7440-39-3
Ti	x	7440-32-6
Sr	x	7440-24-6

L138 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:639158 HCAPLUS

DN 133:216543

TI Fabrication of high-density and low-power **flash memories** with high capacitive-coupling ratio

IN Wu, Shye-lin

PA Texas Instruments - Acer Incorporated, Taiwan

SO U.S., 9 pp., Cont.-in-part of U.S. Ser. No. 36,038. CODEN: USXXAM

DT Patent

LA English

FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6117756	A	20000912	US 1999-336869	19990618
PRAI	US 1998-36038	A2	19980306		

AB The method includes the following steps. At first, a semiconductor substrate with an isolation region formed thereon is provided. The semiconductor substrate has a pad oxide layer and a first nitride layer formed thereon. A portion of the first nitride layer and a portion of the pad oxide layer are removed to define a gate region. A first oxide layer is formed and then a sidewall structure is formed. The semiconductor substrate is doped with first type dopants. A first thermal process is performed to form a **second oxide layer** and to drive in the first type dopants. The sidewall structure and the first nitride layer are then removed, and a first conductive layer is then formed over the substrate. A doping process is performed to dope the pad oxide layer, the first oxide layer, and the **second oxide layer** by implanting second type dopants through the first conductive layer. A second thermal process is performed and a portion of the first conductive layer is removed to define a floating gate. A dielec. layer is formed over the semiconductor substrate and a second conductive layer is then formed thereon as a control gate.

IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **11105-01-4**, Silicon nitride oxide **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(fabrication of high-d. and low-power **flash memories** with high capacitive-coupling ratio)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS

CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 11105-01-4 HCAPLUS

CN Silicon nitride oxide (9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 12033-89-5 HCAPLUS

L129 ANSWER 15 OF 22 HCAPLUS COPYRIGHT 2002 ACS

AN 1998:683733 HCAPLUS

DN 130:9241

TI **Tunneling** leakage current in ultrathin (<4 nm) nitride/oxide **stack dielectrics**

AU Shi, Ying; Wang, Xiewen; Ma, T. P.

CS Center for Microelectronic Materials and Structures and the Department of Electrical Engineering, Yale University, New Haven, CT, 06520, USA

SO IEEE Electron Device Lett. (1998), 19(10), 388-390
CODEN: EDLEDZ; ISSN: 0741-3106

PB Institute of Electrical and Electronics Engineers

DT Journal

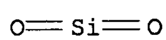
LA English

AB The leakage current in high-quality ultrathin Si nitride/oxide (N/O) **stack dielec.** is calcd. based on a model of 1-step electron tunneling through both the nitride and the oxide layers. The tunneling leakage current in the N/O **stack** is substantially lower than that in the oxide layer of the same equiv. oxide thickness (EOT). The theor. leakage current in N/O **stack** is a strong function of the nitride/oxide EOT ratio: in the direct tunneling regime, the leakage current decreases monotonically as the N/O ratio increases, while in the **Fowler-Nordheim** regime the lowest leakage current is realized with a N/O EOT ratio of 1: 1. Due to the asymmetry of the N/O barrier shape, the leakage current under substrate injection is higher than that under gate injection, although such a difference becomes smaller in the lower voltage regime. Exptl. data obtained from high quality ultrathin N/O **stack dielecs.** agree well with calcd. results.

IT **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(tunneling leakage current in ultrathin nitride/oxide **stack dielecs.**)

RN 7631-86-9 HCAPLUS

CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 HCAPLUS

CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L129 ANSWER 18 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:279323 HCAPLUS
DN 126:349967
TI Novel **stacked** capacitor with high **dielectric** constant (Ba, Sr)TiO3 films using chemical vapor deposition
AU Kawahara, Takaaki; Yamamuka, Mikio; Horikawa, Tsuyoshi; Yuuki, Akimasa; Ono, Kouichi
CS Adv. Technol. R and D Cent., Mitsubishi Electr. Corp., Amagasaki, 661, Japan
SO Mitsubishi Denki Giho (1997), 71(3), 337-342
CODEN: MTDNAF; ISSN: 0369-2302
PB Mitsubishi Denki Gihosha
DT Journal; General Review
LA Japanese
AB A review with 5 refs. The manuf. of gigabit-scale dynamic random access **memory** (DRAM) requires that a capacitance of .apprx.25 fF for a **single cell** be realized on a 0.2 .mu.m-high **stacked** capacitor structure using high **dielec**. const. (Ba, Sr)TiO3 films. Chem. vapor deposition (CVD) plays a key role in fabricating such capacitors due to its excellent step coverage, high deposition rate and compn. controllability. The authors have developed an original liq. source vaporization system and achieved excellent step coverage of about 80% at the low temp. of 420.degree. by incorporating the source materials of Ba(DPM)2, Sr(DPM)2, and TiO(DPM)2 dissolved in THF. They have also developed a CVD process that meets the elec. requirements for producing capacitors for 1 Gb DRAMs.
IT **37303-24-5**, Barium strontium titanium oxide (Ba, Sr)TiO3
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**stacked** capacitors with high **dielec**. const. (Ba Sr)TiO3 films fabricated using chem. vapor deposition)
RN 37303-24-5 HCAPLUS
CN Barium strontium titanium oxide ((Ba,Sr)TiO3) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	3	17778-80-2
Ba	0 - 1	7440-39-3
Ti	1	7440-32-6
Sr	0 - 1	7440-24-6

L78 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1996:485905 HCAPLUS
DN 125:130070
TI Semiconductor **flash** EEPROM memory devices by **channel hot electron injection**
IN Koyama, Takashi; Nara, Akira
PA Hitachi Ltd, Japan; Hitachi Tobu Semiconductor Ltd
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM G11C016-06
ICS G11C029-00; H01L021-8247; H01L029-788; H01L029-792
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08138393	A2	19960531	JP 1994-298784	19941108

AB The title ROM devices comprise non-volatile memory cell array each provided on cross points of word/bit wires, a 1st load MOSFET for selectively transferring write-in voltage for selective word wire for single write-in mode, and a 2nd load MOSFET for transferring write-in voltage for all word wires in the array for simultaneous write-in mode. The arrangement gives the devices an easy testing and provides the devices with simultaneous write-in function for **channel hot electron injection** system.
ST **flash** EEPROM **channel hot electron injection**; semiconductor read only memory cell array; control floating gate memory cell array
IT Memory devices
(read-only, semiconductor; semiconductor **flash** EEPROM memory devices by **channel hot electron injection**)

L78 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:102773 HCAPLUS
TI Self-convergent programming scheme for multilevel P-channel **flash** memory
AU Shen, Shih-Jye; Yang, Ching-Song; Wang, Yen-Sen; Hsu, Charles Ching-Hsiang
CS Microelectronics Laboratory, Semiconductor Technology & Application Research (STAR) Group, Department of Electrical Engineering, National Tsing-Hua University, Hsin-Chu, 300, Taiwan
SO Jpn. J. Appl. Phys., Part 1 (2000), 39(1), 1-7
CODEN: JAPNDE; ISSN: 0021-4922
PB Japanese Journal of Applied Physics
DT Journal
LA English
AB We propose a novel operation scheme for multilevel p-channel **flash** memory cell with a self-convergent programming process. By utilizing the simultaneous Fowler-Nordheim electron tunneling out of floating gate and **channel hot electron injection** into floating gate, the threshold voltage of memory cell can be converged to a specific value. The gate pulse level can be varied to result in different converged threshold voltages such that multilevel can be achieved. Owing to the nature of self-convergence, the possibility of eliminating or reducing the verification operation in multilevel applications increases considerably by using the proposed scheme. In this study the reliability considerations of this programming technique for long-term operations are also addressed.

L135 ANSWER 3 OF 11 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:891598 HCAPLUS
DN 134:50166
TI Method of forming a composite interpoly gate dielectric for nonvolatile semiconductor device
IN Bui, Nguyen Duc
PA Advanced Micro Devices, Inc., USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

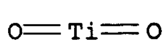
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6163049	A	20001219	US 1998-170061	19981013
	US 2001015456	A1	20010823	US 2000-725843	20001130
PRAI	US 1998-170061	A3	19981013		

AB The as-deposited thickness of at least one of the oxide layers of a composite ONO dielec. film between a floating gate and a control gate of a nonvolatile semiconductor device is deposited to a sufficient thickness such that, after the top oxide layer is cleaned, the control gate is spaced apart from the floating gate a distance corresponding to at least a min. design data retention. Deposition is facilitated by forming one or more oxide layers at a thickness greater than the design rule by employing a relatively **high dielec**. const. material for the oxide layer or layers, such as Al oxide, Ti oxide or Ta oxide. In this way, the capacitance of the ONO film between the floating gate and the control gate is maintained per design rule, avoiding a change in operating voltage. Embodiments include depositing a relatively thick top oxide layer to enable thorough cleaning without adversely reducing the total thickness of the ONO stack and, hence, achieving design data retention.
IT **1314-61-0**, Tantalum pentoxide **1344-28-1**, Aluminum oxide, processes **12033-89-5**, Silicon nitride, processes **13463-67-7**, Titania, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in forming composite interpoly gate dielec. for nonvolatile semiconductor device)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 1344-28-1 HCAPLUS
CN Aluminum oxide (Al2O3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 13463-67-7 HCAPLUS
CN Titanium oxide (TiO2) (8CI, 9CI) (CA INDEX NAME)



L78 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:161048 HCAPLUS
DN 130:290096
TI Low voltage, low current, high speed program step split gate cell with ballistic direct injection for EEPROM/**Flash**
AU Ogura, S.; Hori, A.; Kato, J.; Yamanaka, M.; Odanaka, S.; Fujimoto, H.; Akamatsu, K.; Ogura, T.; Kojima, M.; Kotani, H.
CS Halo LSI Inc., Wappingers Falls, NY, USA
SO Tech. Dig. - Int. Electron Devices Meet. (1998) 987-990
CODEN: TDIMD5; ISSN: 0163-1918
PB Institute of Electrical and Electronics Engineers
DT Journal
LA English
CC 76-14 (Electric Phenomena)
AB By dissocg. from the conventional planar Nch FET structure, a new step split channel device with a new mechanism of ballistic channel hot electron (CHE) injection promises viability in future EEPROM/**Flash** applications. The new non-planar device exhibits fast program of .apprx.100ns, at a max. internal voltage of 5V and at low currents of less than 10.mu.A.
ST split gate cell ballistic direct injection EEPROM **flash**
IT EEPROM devices
Memory devices
(low voltage low current high speed program step split gate cell with ballistic direct injection for EEPROM/**Flash**)
IT Hot electrons
(new step split channel device with new mechanism of ballistic **channel hot electron injection** for EEPROM/**flash** applications)

L112 ANSWER 17 OF 25 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:167123 HCAPLUS
DN 132:201894
TI **Stack** gate **flash memory** cell featuring symmetric self-aligned contact structures
IN Su, Hung-Der; Lin, Chrong-Jung; Chen, Jong; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6037223	A	20000314	US 1998-177342	19981023

AB A process for fabricating a **flash memory** cell featuring self-aligned contact structures overlying and contacting self-aligned **source**, and self-aligned **drain** regions located between **stack** gate structures has been developed. The **stack** gate structures located on an underlying silicon dioxide **tunnel** oxide layer comprise: a capping insulator shape; a polysilicon **control gate** shape; an inter-polysilicon **dielec**. shape; and a polysilicon **floating gate** shape. The use of self-aligned contact structures and self-aligned **source** regions allows increased cell densities to be achieved.
IT **7440-21-3**, Silicon, uses **7631-86-9**, Silicon dioxide, uses
RL: DEV (Device component use); USES (Uses)
(**stack** gate **flash memory** cell featuring sym. self aligned contact structures)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

L77 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:6393 HCAPLUS
DN 136:78257
TI EEPROM with high channel hot carrier injection efficiency
IN Kusunoki, Shigeru; Oda, Hidekazu
PA Mitsubishi Denki K. K., Japan
SO U.S., 48 pp., Cont. -in-part of U. S. Ser. No. 283,863, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6335549	B1	20020101	US 1996-622327	19960326
	JP 07130885	A2	19950519	JP 1993-274695	19931102
PRAI	JP 1993-274695	A	19931102		
	US 1994-283863	B1	19940801		

AB A semiconductor memory device and a method of manufg. the same improves an efficiency of injection of channel hot electrons while suppressing injection of drain avalanche hot carriers. In the semiconductor memory device, a 1st nitrided oxide film (RNO film) contg. a 1st content of H is formed at a drain avalanche hot carrier injection region. Thereby, injection of drain avalanche hot carriers is effectively suppressed during a data writing operation. A 2nd nitrided oxide film (NO film) contg. a 2nd content of H larger than the 1st content is formed at a **channel hot electron injection** region. Thereby, an efficiency of injection of channel hot electrons is improved during the data writing operation.
IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(EEPROM with high channel hot carrier injection efficiency)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7664-41-7**, Ammonia, processes
RL: PEP (Physical, engineering or chemical process); RCT (Reactant); PROC (Process); RACT (Reactant or reagent)
(nitridation atm.; EEPROM with high channel hot carrier injection efficiency)
RN 7664-41-7 HCAPLUS
CN Ammonia (8CI, 9CI) (CA INDEX NAME)

NH_3

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(nitrided; EEPROM with high channel hot carrier injection efficiency)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

$O{=}Si{=}O$

IT **7440-21-3**, Polysilicon, uses

L77 ANSWER 2 OF 2 HCAPLUS
AN 2000:201132 HCAPLUS
DN 132:230700
TI **Flash** EEPROM device employing polysilicon sidewall spacer as an erase gate
IN Chang, Ming-bing
PA USA
SO U.S., 16 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6043530	A	20000328	US 1998-60673	19980415
	US 6261907	B1	20010717	US 1999-453395	19991203
PRAI	US 1998-60673	A3	19980415		

AB A **Flash** EEPROM cell employing a sidewall polysilicon spacer as an erase gate. The cell is programmed by source side **channel hot electron injection** and erased by poly-to-poly tunneling through a poly tunnel oxide between the floating gate and the erase gate. The floating gate is defined by the control gate sidewall spacer which is formed before the floating gate poly self-aligned etch step. The polysilicon sidewall spacer erase gate is formed after growing a poly tunnel oxide on the sidewall of the floating gate poly. Since the poly tunnel oxide thickness is minimized, a fast programming with a low power consumption can be achieved. By using poly-to-poly tunneling erase scheme, a deep source junction is not used and cell size can be significantly reduced. Furthermore, a large sector of cells can be erased simultaneously without a power consumption concern and further Vcc scaling becomes possible.
IT **7440-21-3**, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(**flash** EEPROM device employing polysilicon sidewall spacer as erase gate)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L89 ANSWER 1 OF 7 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:597602 HCAPLUS
DN 135:161096
TI Nonvolatile semiconductor **flash memory** device
IN Kawaguchi, Tsutomu; Fukazu, Shigemitsu
PA Denso Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001223278	A2	20010817	JP 2000-30366	20000208

AB The invention relates to a nonvolatile semiconductor **memory** device, i.e., **F-N tunneling flash memory** or EEPROM, wherein the dual gate layout **minimizes** the rewrite **voltage** without lessoning the rewrite speed.
IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(nonvolatile semiconductor **flash memory** device)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

L102 ANSWER 1 OF 23 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:567927 HCAPLUS
DN 135:311975
TI Materials characterization of ZrO2-SiO2 and HfO2-SiO2 binary oxides deposited by chemical solution deposition
AU Neumayer, D. A.; Cartier, E.
CS IBM, T. J. Watson Research Center, Yorktown Heights, NY, 10598, USA
SO Journal of Applied Physics (2001), 90(4), 1801-1808
CODEN: JAPIAU; ISSN: 0021-8979
PB American Institute of Physics
DT Journal
LA English
AB The thermal stability, microstructure, and elec. properties of xZrO2.cntdot.(100-x)SiO2 (ZSO) and xHfO2.cntdot.(100-x)SiO2 (HSO) (x = 15%, 25%, 50%, and 75%) binary oxides were evaluated to help assess their suitability as a replacement for SiO2 gate dielecs. in complementary metal-oxide-semiconductor transistors. The films were prepd. by chem. soln. deposition using a soln. prepd. from a mixt. of Zr, Hf, and Si butoxyethoxides dissolved in butoxyethanol. The films were spun onto SiOxNy coated Si wafers and furnace annealed at 500-1200.degree. in O for 30-60 min. The microstructure and elec. properties of ZSO and HSO films were examd. as a function of the Zr/Si and Hf/Si ratio and annealing temp. The films were characterized by x-ray diffraction, mid- and far-FTIR, Rutherford backscattering spectroscopy, and Auger electron spectroscopy. At ZrO2 or HfO2 concns. .gtoreq.50%, phase sepn. and crystn. of tetragonal ZrO2 or HfO2 were obsd. at 800.degree.. At ZrO2 or HfO2 concns. .ltoreq. 25%, phase sepn. and crystn. of tetragonal ZrO2 or HfO2 were obsd. at 1000.degree.. As the annealing temp. increased, a progressive change in microstructure was obsd. in the FTIR spectra. Addnl., the FTIR spectra suggest that HfO2 is far more disruptive of the SiO2 network than ZrO2 even at HfO2 concns. .ltoreq.25%. The dielec. consts. of the 25%, 50%, and 75% ZSO films were measured and are less than the linear combination of ZrO2 and SiO2 dielec. consts. The dielec. const. also increases with increasing ZrO2 content. The dielec. const. also is annealing temp. dependent with larger dielec. consts. obsd. in non-phase sepd. films. The Clausius-Mossoti equation and a simple capacitor model for a phase sepd. system fit the data with the prediction that to achieve a dielec. const. larger than 10 doping concns. of ZrO2 would have to be >70[percent].

L102 ANSWER 8 OF 23 HCAPLUS

AN 1987:206187 HCAPLUS
DN 106:206187
TI Deposition and properties of ultra-thin high dielectric constant insulators
AU Roberts, Stanley; Ryan, James G.; Martin, Dale W.
CS Gen. Technol. Div., IBM Corp., Essex Junction, VT, 05452, USA
SO ASTM Spec. Tech. Publ. (1987), 960(Emerging Semicond. Technol.), 137-49
CODEN: ASTTA8; ISSN: 0066-0558
DT Journal
LA English
AB Exploratory studies were carried out with reactively sputtered thin films of several transition metal oxides and co-sputtered mixts. with SiO2. Good insulation behavior is obsd. following post-deposition oxidn. anneals. Best overall elec. properties are obsd. with mixts. of HfO2 and SiO2, in combination with addnl. layers of thermal SiO2 and chem.-vapor deposited (CVD) Si3N4. Significant redn. in dielec. const. is obsd. with all the transition metal oxides with sub-30-nm films. High capacitance with stacks contg. thermal SiO2, mixts. of HfO2 and SiO2, and CVD Si3N4 may be due to a charge storage mechanism.
IT **1314-61-0**, Tantalum pentoxide **7631-86-9**, properties
12033-89-5, Silicon nitride (Si3N4), properties **12055-23-1**
, Hafnium dioxide **108356-79-2**
RL: USES (Uses)
(sputter deposition and phys. properties of insulating film structures contg.)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 12055-23-1 HCAPLUS
CN Hafnium oxide (HfO2) (8CI, 9CI) (CA INDEX NAME)

O═Hf═O

RN 108356-79-2 HCAPLUS
CN Hafnium oxide silicate (Hf4O6(SiO4)) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	6	17778-80-2
O4Si	1	17181-37-2
Hf	4	7440-58-6

L112 ANSWER 1 OF 25 HCAPLUS
AN 2001:755763 HCAPLUS
DN 135:297067
TI Process for a snap-back **flash** EEPROM cell
IN Yeh, Juang-Ker; Lee, Jian-Hsing; Peng, Kuo-Reay; Ho, Ming-Chou
PA Taiwan Semiconductor Manufacturing Company, Taiwan
SO U.S., 13 pp., Division of U.S. Ser. No. 17,408, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6303454	B1	20011016	US 2000-590849	20000609
PRAI	US 1998-17408	B3	19980202		

AB The present invention provides method to fabricate a snap-back **flash** EEPROM device. The method begins by forming a gate structure on a substrate. The gate structure comprises: a **tunnel** oxide layer, a **floating gate**, integrate **dielec** . layer, and a **control gate**. A **drain** is formed adjacent to the gate structure by a masking and ion implant process. Next, a **source** side doped region is formed adjacent to and under a portion of the gate structure by an masking and ion implant process. Spacers are now formed on the sidewalls of the gate structure. A **source** is formed overlapping portion of the side **source** doped region and adjacent to the spacers. The side **source** doped region has a lower dopant concn. than the **source**. This method forms a snap-back **memory** cell in which the side **source** doped region is used to **apply** a high **voltage** to operate the EEPROM cell in a snap-back erase mode.

IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **11105-01-4**, Silicon nitride oxide
RL: DEV (Device component use); USES (Uses)
(process for a snap-back **flash** EEPROM cell)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 11105-01-4 HCAPLUS
CN Silicon nitride oxide (9CI) (CA INDEX NAME)

L112 ANSWER 2 OF 25 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:352249 HCAPLUS
DN 134:335380
TI Design and fabrication of a split gate **flash memory** cell
IN Chen, Chih Ming
PA Taiwan Semiconductor Manufacturing Corporation, Taiwan
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6232180	B1	20010515	US 1999-347203	19990702

AB A split gate **flash memory** cell formed in a semiconductor substrate is disclosed. The **memory** cell comprises: a deep n-well formed in the substrate; a p-well formed in the deep n-well; a select gate structure formed on the p-well, the select gate structure comprising a **stack** of a gate oxide, a polysilicon layer, and a cap oxide; a **tunnel** oxide layer formed on the p-well, the **tunnel** oxide adjacent to the **control gate** structure; a **floating gate** formed over the select gate structure and extending over at least a portion of the **tunnel** oxide layer; a **source** formed in the p-well, the **source** formed adjacent to the **floating gate**; and a **drain** formed in the p-well, the **drain** formed adjacent to the select gate structure. The **memory** cell is programmed by **source** side channel hot electron and is erased using channel erasing to improve cycling endurance.

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(design and fabrication of a split gate **flash memory** cell)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

$O=Si=O$

IT **7440-21-3**, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; design and fabrication of a split gate **flash memory** cell)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L112 ANSWER 25 OF 25 HCAPLUS COPYRIGHT 2002 ACS
AN 1984:16337 HCAPLUS
DN 100:16337
TI Nonvolatile EPROM and EEPROM with increased efficiency
IN Harari, Eliyahou
PA USA
SO U.S., 18 pp. Cont.-in-part of U.S. 4,328,565.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4409723	A	19831018	US 1980-184739	19800908
	GB 2073487	A	19811014	GB 1981-8759	19810320
	GB 2073487	B2	19840404		
	DE 3117719	C2	19880428	DE 1981-3117719	19810505
PRAI	US 1980-137764		19800407		
	US 1980-184739		19800908		

AB A nonvolatile EPROM (elec. programmable and UV erasable), or EEPROM (elec. programmable and elec. erasable) cell has high d., high injection charge d. per **applied** write **voltage**, high drive capacity, effective injection charge control and writing, a large read threshold window, a large read current per applied access volt, sep. channel positions for access and for injection charge, and elimination of low-level parasitic currents during read or write. The **drain** -to-**floating gate** capacitance of the **memory** array is deliberately maximized, and the **drain**-turn-on condition is avoided by essentially decoupling the **floating gate** from the **source** diffusion. The devices have **floating gates** capable of attaining a higher capacitively coupled voltage than previously attainable. A thin **tunneling dielec**. (e.g. SiO_2 or Si_3N_4) can be used and the devices can then be easily reprogrammed by dropping the potential on the **control gate** to a low level (particularly -20 V) while holding the **source**, **drain**, and substrate at zero-volts. A region of thin oxide is formed underneath a portion of the **floating gate** over the channel region. This region of thin oxide allows a **floating gate** to be reprogrammed using electron **tunneling** with a relatively high voltage pulse supplied to the **floating gate** through either its **drain** capacitance or **control gate** capacitance. The process sequence is described.

IT **7440-42-8**, uses and miscellaneous
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(implantation doping with, of silicon **memory** devices)
RN 7440-42-8 HCAPLUS
CN Boron (8CI, 9CI) (CA INDEX NAME)

B

IT **7631-86-9**, uses and miscellaneous **12033-89-5**, uses and miscellaneous
RL: USES (Uses)
(in **memory** devices elec. programmable and elec. programmable and erasable, with increased efficiency)
RN 7631-86-9 HCAPLUS

CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7440-21-3**, uses and miscellaneous
RL: DEV (Device component use); USES (Uses)
(**memory** devices, elec. programmable and elec. programmable and erasable, with increased efficiency)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L112 ANSWER 24 OF 25 HCAPLUS

AN 1996:71250 HCAPLUS

DN 124:103948

TI Semiconductor **memory** devices and **memory** arrays and manufacture thereof

PA Nippon Precision Circuits K. K., Japan

SO Jpn. Kokai Tokkyo Koho, 16 pp.
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07302853	A2	19951114	JP 1995-67670	19950327
	JP 2928986	B2	19990803		
	US 5635416	A	19970603	US 1995-474259	19950607
	US 5773861	A	19980630	US 1995-559800	19951117
	US 6331724	B1	20011218	US 1997-997407	19971223
PRAI	US 1994-237761	A	19940504		
	US 1995-559800	A1	19951117		

AB The title process comprises sequential formation of a 1st **dielec**. **tunneling** (e.g., from SiO2), a 1st semiconductor (e.g., polycryst. Si), and a 1st nitride layer on the substrate, selective removal of the 1st nitride and the 1st semiconductor layer to expose the substrate surface, formation of a 1st insulating field regions (e.g., from SiO2), removal of the nitride layer, implantation of an impurity through the 1st semiconductor, the 1st **dielec**., and the 1st insulating field film, deposition of a 2nd semiconductor layer (e.g., polycryst. Si, for **floating gate** with the 1st semiconductor layer) on the 1st semiconductor layer and the 1st insulating field film, doping of the 2nd semiconductor layer and selective etching thereof to expose the center portions of the 1st insulating field film, sequential deposition of a 2nd **dielec**. and a 3rd semiconductor (e.g., polycryst. or amorphous Si, for **control gate**) on the 2nd semiconductor layer, doping of the 3rd semiconductor layer, and ion implantation into the substrate to form the **source-drain** regions, esp. for elec. erasable programmable ROM.

IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(prepn. of **stacked** silicon gate cell structures with **tunneling** oxide layers for **memory** devices)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS

CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 12033-89-5 HCAPLUS

L130 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:68097 HCAPLUS
TI Nonvolatile semiconductor **memory**. [Machine Translation].
IN Iwahashi, Hiroshi
PA Toshiba Micro Electronics K. K., Japan; Toshiba Corp.
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM G11C016-02
ICS G11C014-00; G11C015-04; G11C016-04; H01L027-115; H01L021-8247; H01L029-788; H01L029-792
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000030471	A2	20000128	JP 1998-198337	19980714

AB [Machine Translation of Descriptors]. The many-valued data is made the book changing possible in the nonvolatile semiconductor **memory** which designates the MOS transistor which possesses the elec. charge accumulation layer in the gate insulator as the **memory** cell. Accumulates the electron to the elec. charge .apprx. laminate of drain side of the MOS transistor which becomes the **memory** cell, or to the elec. charge .apprx. laminate of source side of the MOS transistor accumulates the electron, or to both of the elec. charge .apprx. laminate of drain side and source side of the MOS transistor accumulates the electron, or to the elec. charge .apprx. laminate of drain side or source side of the MOS transistor does not accumulate the electron, or remembers the data of 2 bits in the MOS transistor with **four states**.

L130 ANSWER 3 OF 3 HCAPLUS

AN 1997:124299 HCAPLUS
DN 126:138810
TI Nonvolatile semiconductor **memory**
IN Mori, Seiichi
PA Tokyo Shibaura Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L021-8247
ICS H01L029-788; H01L029-792; G11C016-02; G11C016-04; H01L027-115
CC 76-14 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08316343	A2	19961129	JP 1995-118093	19950517

AB The invention relates to a floating-gate **four-state** nonvolatile semiconductor **memory** capable of storing two bites of information in one **memory**, wherein the neutral threshold voltage, i.e. the threshold voltage when no charge is stored on the floating-gate, is selected between the 2nd- and 3rd state for the extension of the charge-maintaining period.
ST nonvolatile semiconductor **memory** multistate
IT Semiconductor **memory** devices
(multistate nonvolatile semiconductor **memory** device)

L129 ANSWER 1 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:792284 HCAPLUS
DN 135:326135
TI Method of forming high k tantalum pentoxide Ta2O5 instead of ONO **stacked** films to increase coupling ratio and improve reliability for **flash memory** devices
IN Au, Kenneth Wo-wai; Chang, Kent Kuohua; Chi, David
PA Advanced Micro Devices, Inc., USA
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6309927	B1	20011030	US 1999-263983	19990305
	US 2001046738	A1	20011129		

AB In one embodiment, the present invention relates to a method of forming a **flash memory** cell, involving the steps of forming a tunnel oxide on a substrate; forming a 1st polysilicon layer over the tunnel oxide; forming an insulating layer over the 1st polysilicon layer, the insulating layer comprising an oxide layer over the 1st polysilicon layer, and a Ta pentoxide layer over the oxide layer, in which the Ta pentoxide layer is made by CVD at a temp. from .apprx.200.degree. to .apprx.650.degree. using an org. Ta compd. and an O compd., and heating in an N2O atm. at a temp. from .apprx.700.degree. to .apprx.875.degree.; forming a 2nd polysilicon layer over the insulating layer; etching at least the 1st polysilicon layer, the 2nd polysilicon layer and the insulating layer, thereby defining at least one **stacked** gate structure; and forming a source region and a drain region in the substrate, thereby forming at least **one memory cell**.
IT **1314-61-0**, Tantalum oxide (Ta2O5) **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride (Si3N4), uses **12627-41-7**, Tungsten silicide
RL: DEV (Device component use); USES (Uses)
(method of forming high k tantalum pentoxide Ta2O5 instead of ONO **stacked** films to increase coupling ratio and improve reliability for **flash memory** devices)
RN 1314-61-0 HCAPLUS
CN Tantalum oxide (Ta2O5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
RN 12627-41-7 HCAPLUS
CN Tungsten silicide (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number

L129 ANSWER 14 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:388532 HCAPLUS
DN 133:11778
TI LPCVD oxide and RTA for top oxide of ONO film to improve reliability for **flash memory** devices
IN Chang, Kent Kuohua; Chi, David; Sun, Chin-Yang
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp., Cont.-in-part of U.S. Ser. No. 98,292.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6074917	A	20000613	US 1998-189227	19981111
	US 6063666	A	20000516	US 1998-98292	19980616
PRAI	US 1998-98292	A2	19980616		

AB In one embodiment, the present invention relates to a method of forming a **flash memory** cell, involving the steps of forming a tunnel oxide on a substrate; forming a first polysilicon layer over the tunnel oxide; forming an insulating layer over the first polysilicon layer, the insulating layer comprising a first oxide layer over the first polysilicon layer, a nitride layer over the first oxide layer, and a second oxide layer over the nitride layer, wherein the second oxide layer is made by forming the second oxide layer by low pressure chem. vapor deposition at a temp. from about 600-850.degree. using SiH4 and N2O and annealing in an N2O atm. at a temp. from about 700-950.degree.; forming a second polysilicon layer over the insulating layer; etching at least the first polysilicon layer, the second polysilicon layer and the insulating layer, thereby defining at least one **stacked** gate structure; and forming a source region and a drain region in the substrate, thereby forming at least **one memory cell**.
IT **7440-21-3**, Silicon, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(LPCVD oxide and RTA for top oxide of ONO film to improve reliability for **flash memory** devices)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7631-86-9P**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(LPCVD oxide and RTA for top oxide of ONO film to improve reliability for **flash memory** devices)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

L129 ANSWER 19 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1994:618994 HCAPLUS
DN 121:218994
TI Transient behavior and **memory** effect of a PbZrxTi1-xO3/YBa2Cu3O7-x three-terminal device
AU Lin, H.; Wu, N. J.; Xie, K.; Li, X. Y.; Ignatiev, A.
CS Texas Cent. Superconductivity, Univ. Houston, Houston, TX, 77204-5507, USA
SO Appl. Phys. Lett. (1994), 65(8), 953-5
CODEN: APPLAB; ISSN: 0003-6951
DT Journal
LA English
AB The transient behavior of a ferroelec. PbZrxTi1-xO3 and superconducting YBa2Cu3O7-x three-terminal device was studied. **Four-state** behavior, i.e., two polarization states of the PbZrxTi1-xO3 gate and superconducting and normal states of the YBa2Cu3O7-x layer, was obsd. The biased superconducting channel can be switched from superconducting state to the normal state by the flowing charge during the polarization switching of the PbZrxTi1-xO3 gate. The nonvolatility of this device based on the different polarization states of the ferroelec. gate also was demonstrated.
IT **12626-81-2**, Lead titanium zirconium oxide (PbTi0-1Zr0-1O3)
109064-29-1D, Barium copper yttrium oxide (Ba2Cu3YO7), oxygen-deficient
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(transient behavior and **memory** effect of lead titanium zirconium oxide/barium copper yttrium oxide three-terminal device)
RN 12626-81-2 HCAPLUS
CN Lead titanium zirconium oxide (Pb(Ti,Zr)O3) (9CI) (CA INDEX NAME)

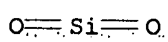
Component	Ratio	Component Registry Number
O	3	17778-80-2
Zr	0 - 1	7440-67-7
Ti	0 - 1	7440-32-6
Pb	1	7439-92-1

RN 109064-29-1 HCAPLUS
CN Barium copper yttrium oxide (Ba2Cu3YO7) (9CI) (CA INDEX NAME)

Component	Ratio	Component Registry Number
O	7	17778-80-2
Y	1	7440-65-5
Cu	3	7440-50-8
Ba	2	7440-39-3

L129 ANSWER 22 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 1986:80358 HCAPLUS
DN 104:80358
TI A 100 .ANG. thick **stacked** silica/silicon nitride/silica
dielectric layer for **memory** capacitor
AU Watanabe, T.; Menjoh, A.; Mochizuki, T.; Shinozaki, S.; Ozawa, O.
CS Semicond. Device Eng. Lab., Toshiba Corp., Kawasaki, 210, Japan
SO Annu. Proc., Reliab. Phys. [Symp.] (1985), 23rd 18-23
CODEN: ARLPBI; ISSN: 0099-9512
DT Journal
LA English
AB The reliability was studied of SiO2-Si3N4-SiO2 film **stacks** in
capacitor **memories**. The **leakage currents**
and flat-band **voltages** are given. The **dielec.**
breakdown is described. These structures have very low failure rates. A
Fowler-Nordheim tunneling model which takes into account
trapping effects satisfactorily describes the results.
IT **12033-89-5**, uses and miscellaneous
RL: USES (Uses)
(**memory** capacitor from **dielec.** layers of silica
and)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7631-86-9**, uses and miscellaneous
RL: USES (Uses)
(**memory** capacitor from **dielec.** layers of silicon
nitride and)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)



IT **7440-21-3**, uses and miscellaneous
RL: PRP (Properties)
(**memory** capacitor from phosphorus-doped polycryst.)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L138 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:388532 HCAPLUS
DN 133:11778
TI LPCVD oxide and RTA for top oxide of ONO film to improve reliability for **flash memory** devices
IN Chang, Kent Kuohua; Chi, David; Sun, Chin-Yang
PA Advanced Micro Devices, Inc., USA
SO U.S., 8 pp., Cont.-in-part of U.S. Ser. No. 98,292.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6074917	A	20000613	US 1998-189227	19981111
	US 6063666	A	20000516	US 1998-98292	19980616
PRAI	US 1998-98292	A2	19980616		

AB In one embodiment, the present invention relates to a method of forming a **flash memory** cell, involving the steps of forming a tunnel oxide on a substrate; forming a first polysilicon layer over the tunnel oxide; forming an insulating layer over the first polysilicon layer, the insulating layer comprising a first oxide layer over the first polysilicon layer, a nitride layer over the first oxide layer, and a **second oxide layer** over the nitride layer, wherein the **second oxide layer** is made by forming the **second oxide layer** by low pressure chem. vapor deposition at a temp. from about 600-850.degree. using SiH4 and N2O and annealing in an N2O atm. at a temp. from about 700-950.degree.; forming a second polysilicon layer over the insulating layer; etching at least the first polysilicon layer, the second polysilicon layer and the insulating layer, thereby defining at least one stacked gate structure; and forming a source region and a drain region in the substrate, thereby forming at least one memory cell.
IT **7440-21-3**, Silicon, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(LPCVD oxide and RTA for top oxide of ONO film to improve reliability for **flash memory** devices)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **7631-86-9P**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(LPCVD oxide and RTA for top oxide of ONO film to improve reliability for **flash memory** devices)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

L144 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:524009 HCAPLUS
DN 135:85768
TI Structure of a **flash memory** device
IN Lee, Chien-hsing
PA United Microelectronics Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6262917	B1	20010717	US 2000-534668	20000324
PRAI	TW 1999-88118300	A	19991022		

AB A **flash memory** device is described. A **gate** oxide layer is situated on a **substrate** next to a trench and a **floating gate** is located on the gate oxide layer. A **source** region is located in the **substrate** at the bottom of the trench and a **drain** region is located on a side of the floating gate. A **dielec.** layer is on the floating gate, the gate oxide layer and the trench. A control gate is located on the **dielec.** layer.

IT **7440-21-3P**, Polysilicon, uses
RL: DEV (Device component use); PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(floating oxide gate **dielec.** layer structure in **flash memory** device)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L144 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:255887 HCAPLUS
DN 134:260135
TI Method for manufacturing a two-bit flash semiconductor memory device
IN Lee, Robin
PA United Semiconductor Corp., Taiwan; United Microelectronics Corp.
SO U.S., 6 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6214672	B1	20010410	US 1999-428356	19991028

AB A method is presented for manufg. a 2-bit **flash memory**. A substrate has a thin oxide layer, a Si nitride layer and a material layer formed thereon in sequence. An opening is formed in the material layer and the Si nitride layer to expose a portion of the thin oxide layer. A **source/drain** region is formed in the **substrate** beneath the portion of the thin oxide layer exposed by the opening. A 1st **dielec**. layer is formed in the opening. A portion of the material layer and a portion of the Si nitride layer are removed to form a spacer on the sidewall of the 1st **dielec**. layer. The remaining material layer is removed. A portion of the thin oxide layer exposed by the remaining Si nitride layer and the 1st **dielec**. layer is removed. A 2nd **dielec**. layer is formed on a portion of the substrate exposed by the remaining thin oxide layer. A control **gate** is formed over the **substrate**.

IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method for manufg. a two-bit flash semiconductor memory device)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L144 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:222045 HCAPLUS
DN 134:230746
TI **Flash memory** cells having modulation doped heterojunction structure
IN Fastow, Richard
PA Advanced Micro Devices, Inc., USA
SO U.S., 12 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6207978	B1	20010327	US 2000-516472	20000301

AB The **flash memory** device includes a modulation-doped heterostructure formed in a semiconductor **substrate**, a layer of tunnel oxide, a **floating gate**, a layer of **dielec.**, a control **gate** and **source** and **drain** regions formed in the **substrate**.
IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **11148-21-3** **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(**flash memory** cells having modulation doped heterojunction structure)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si_3N_4) (8CI, 9CI) (CA INDEX NAME)

L144 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:874164 HCAPLUS

DN 134:35952

TI Method of fabricating a **flash memory** with a planarized topography

IN Lee, Tzung-han

PA United Microelectronics Corp., Taiwan

SO U.S., 6 pp.
CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6159797	A	20001212	US 1998-137668	19980820
	TW 390028	B	20000511	TW 1998-87109049	19980608
PRAI	TW 1998-87109049	A	19980608		

AB A method of fabricating a **flash memory** includes successive formation of a 1st polysilicon layer, a 1st **dielec**. layer and a hard material layer on a substrate with a tunnelling oxide layer. Then the hard material layer, the 1st **dielec**. layer and the 1st polysilicon layer are defined and the 1st polysilicon layer serves as a floating gate of the **flash memory**. After the step of definition, a **source/drain** region is formed on the **substrate** on the sides of the **floating gate** and an insulating spacer is also formed thereon. An inter-poly **dielec**. layer is then formed over the substrate and CMP was performed to etch back the inter-poly **dielec**. layer, exposing the surface of the hard material layer serving as a stop layer. Next, the hard material layer is removed and the 1st polysilicon layer is doped with impurities. A 2nd **dielec**. layer is formed over the substrate and covers the surface of the 1st polysilicon layer. Subsequently, the 2nd polysilicon layer is formed and defined to serve as a control gate of the **flash memory**.

IT **11105-01-4**, Silicon nitride oxide **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabricating **flash memory** with planarized topog.)

RN 11105-01-4 HCAPLUS

CN Silicon nitride oxide (9CI) (CA INDEX NAME)

L144 ANSWER 10 OF 14 HCAPLUS
AN 2000:10679 HCAPLUS
DN 132:72259
TI **Flash memory** cell with vertical channels and source/drain bus lines
IN Lin, Chrong-Jung; Chen, Shui Hung; Chen, Jong; Kuo, Di-Son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6011288	A	20000104	US 1997-995999	19971222
	US 6066874	A	20000523	US 1999-407108	19990927
PRAI	US 1997-995999		19971222		

AB A vertical memory device on a Si **substrate** comprises a **floating gate** trench in the **substrate**. The walls of the floating gate trench are doped with a threshold implant through the trench surfaces. There is a tunnel oxide layer on the trench surfaces. There is a floating gate electrode in the trench on the outer surfaces of the tunnel oxide layer. There are **source/drain** regions in the **substrate** self-aligned with the **floating gate** electrode. A source line and a drain line are formed above the source region and the drain region, resp. An interelectrode **dielec.** layer overlies the floating gate electrode, the source line, and the drain line, and there is a control gate electrode over the interelectrode **dielec.** layer over the floating gate electrode.

IT **7440-21-3**, Silicon, uses
RL: DEV (Device component use); USES (Uses)
(**flash memory** cell with vertical channels, and source/drain bus lines based on)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(**flash memory** cell with vertical channels, and source/drain bus lines contg.)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

L144 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:671063 HCAPLUS
DN 131:280274
TI Method for forming vertical channels in split-gate **flash memory** cell
IN Lin, Chrong-jung; Hsieh, Chia-ta; Chen, Jong; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5970341	A	19991019	US 1997-988772	19971211
	US 6078076	A	20000620	US 1999-317645	19990524
PRAI	US 1997-988772	A3	19971211		

AB A method of forming a vertical memory split gate **flash memory** device, particularly EEPROM device, on a silicon semiconductor substrate is provided by the following steps. Form a **floating gate** trench hole in the silicon semiconductor **substrate**, the trench hole having trench surfaces. Form a tunnel oxide layer on the trench surfaces, the tunnel oxide layer having outer surfaces. Form a floating gate electrode layer filling the trench hole on the outer surfaces of the tunnel oxide layer. Form **source/ drain** regions in the **substrate** self-aligned with the **floating gate** electrode layer. Pattern the floating gate electrode layer by removing the gate electrode layer from the drain region side of the trench hole. Form a control gate hole therein. Form an interelectrode **dielec.** layer over the top surface of the floating gate electrode, and over the tunnel oxide layer. Form a control gate electrode over the interelectrode **dielec.** layer over the top surface of the floating gate electrode and extending down into the control gate hole in the trench hole.
IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses
RL: DEV (Device component use); USES (Uses)
(formation of vertical channels in split-gate **flash memory** cell)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

L144 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:622366 HCAPLUS
DN 131:236801
TI Forming a vertical-channel **flash memory** cell
IN Lin, Chrong Jung; Chen, Shui-hung; Chen, Jong; Kuo, Di-son
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5960284	A	19990928	US 1997-985647	19971205

AB A vertical memory device on a Si substrate is formed by the following steps. An array of isolation Si oxide structures is formed on the substrate. A **floating-gate** trench is formed in the **substrate** between the Si oxide structures in the array. The sidewalls of the floating-gate trench are doped with a threshold implant through the trench sidewall surfaces. A tunnel oxide layer is formed on the trench sidewall surfaces. A floating gate electrode is formed in the trench on the tunnel oxide layer. **Source/drain** regions are formed in the **substrate** self-aligned with the **floating gate** electrode. An interelectrode **dielec.** layer is formed over the top surface of the floating gate electrode. A control gate electrode is formed over the interelectrode **dielec.** layer. A source line is formed by performing a self-aligned etch followed by a source line implant.

IT **7440-21-3**, Silicon, processes **7631-86-9**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(forming vertical channel **flash memory** cell contg.)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

L144 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2002 ACS
AN 1998:366861 HCAPLUS
DN 129:35219
TI Process for fabricating **flash memory** cells
IN Hsu, Chen-chung
PA United Microelectronics Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5759896	A	19980602	US 1996-669966	19960625

AB A process for fabricating **flash memory** cells that requires lower voltages between the drain and source regions when storing or erasing data, and avoids the punch-through problem assocd. with conventional **flash memory** devices having a high device d., includes forming successively on a Si **substrate** a tunnel oxide layer, a **floating gate** layer, a **dielec**. layer, and a control gate layer. A portion of the tunnel oxide layer is exposed and unshielded. An ion implantation procedure is then applied to the Si **substrate** to form **source** and **drain** regions. Sidewall spacers are then formed on the sidewalls of the control gate layer, the **dielec**. layer, the floating gate layer, and an unexposed portion of the tunnel oxide layer. Finally, an impurity is implanted by inclined ion implantation at an angle of incidence of .apprx.30-40.degree. to form a lightly doped **source** region in the Si **substrate** under the unshielded portion of the tunnel oxide layer.
IT **7440-21-3**, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating **flash memory** cells contg.)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L144 ANSWER 14 OF 14 HCAPLUS

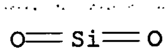
AN 1995:739018 HCAPLUS
DN 123:215661
TI Forming a **flash memory** with high coupling ratio
IN Hong, Gary
PA United Microelectronics Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5432112	A	19950711	US 1994-238873	19940506
	US 5675162	A	19971007	US 1996-641411	19960430
PRAI	US 1994-238873		19940506		
	US 1995-445934		19950522		

AB In forming a **flash memory** device on a semiconductor **substrate** having a **source**, a **drain**, a **dielec**. layer deposited on the **substrate**, and a 1st **floating gate** electrode formed on the **dielec**. layer, a 2nd floating gate electrode is formed on the 1st floating gate electrode, a 2nd **dielec**. layer is deposited on the 1st and 2nd floating gate electrodes, and a control gate electrode is deposited on the 2nd **dielec**. layer, and means for applying a voltage to the control gate electrode. A Si_3N_4 layer is formed on the 1st floating gate electrode and patterned to form an opening to alloy the 2nd floating gate electrode to be deposited on the 1st floating gate electrode.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride (Si_3N_4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in manuf. of **flash memory** with high coupling ratio)

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)



RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si_3N_4) (8CI, 9CI) (CA INDEX NAME)

L147 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:408001 HCAPLUS

DN 134:374996

TI Method of forming a split gate **flash memory** cell with a self-aligned source and drain

IN Lee, Chien-hsing

PA United Microelectronics Corp., Taiwan

SO U.S., 10 pp.
CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6242309	B1	20010605	US 2000-584696	20000601

AB A semiconductor wafer includes a Si **substrate**, at least two **floating gates** positioned on the Si **substrate** and a Si nitride layer positioned on the surface of each floating gate. The method 1st uses a lithog. process and an ion implantation process to form a **drain** in the Si **substrate** between the two **floating gates**. A passivation layer is then formed uniformly on the surface of the Si substrate and the top surface and the sides of the floating gate. An etching process was performed later to form a spacer around each floating gate, the spacers between the floating gate are joined and cover the drain. Finally, an ion implantation process was performed, using the spacers as a hard mask, to form a **source** in the Si **substrate**.

IT **7440-21-3**, Silicon, processes **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method of forming split gate **flash memory** cell with self-aligned source and drain)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS

CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS

CN Silicon nitride (Si_3N_4) (8CI, 9CI) (CA INDEX NAME)

L147 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:784336 HCAPLUS
DN 133:328468
TI Method for manufacturing split-gate **flash memory** cell
IN Wang, Ling-Sung; Chang, Ko-Hsing
PA Worldwide Semiconductor Manufacturing Corp., Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6143606	A	20001107	US 1998-61618	19980416
	JP 2889232	B2	19990510	JP 1998-143654	19980526
PRAI	TW 1997-86119753	A	19971226		

AB In this method for manufg. a split-gate **flash memory** cell, a floating gate and a control **gate** are formed over a **substrate**, and then 1st spacers are formed on the sidewalls of the gate structure. Next, a polysilicon layer is deposited over the **gate** structure and the **substrate**, and 2nd spacers are formed on the sidewalls of the polysilicon layer. A self-aligned ion implantation process is performed, using the 2nd spacers as a mask, implanting ions into the semiconductor **substrate** to form a **drain** region. This maintains the channel length. After removing the 2nd spacers, another ion implantation process is performed to create a **source** region in the semiconductor **substrate**. During the 2nd implantation, the polysilicon layer offers some protection for the semiconductor substrate, maintaining the capacity for tunneling. Finally, a conductive layer is formed over the polysilicon layer, and the conductive layer combined with the polysilicon layer forms the select gate.

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes **12627-41-7**, Tungsten silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for manufg. split-gate **flash memory** cell)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

IT **7440-21-3**, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; method for manufg. split-gate **flash memory** cell)

L147 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:623780 HCAPLUS
DN 133:186733
TI **Flash memory** cell using poly to poly tunneling for erase and its fabrication
IN Leu, Len-Yi
PA Windbond Electronic Corp, Taiwan
SO U.S., 9 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6114723	A	20000905	US 1998-156583	19980918
	US 6365459	B1	20020402	US 2000-528516	20000320
PRAI	US 1998-156583	A3	19980918		

AB An improved split gate **flash memory** cell is disclosed whose floating gate is formed to have a reentrant angle such that its width increases with increased distance from the substrate so as to minimize the possibility of defects in the poly oxide layer overlaying the floating gate. The split gate **flash memory** is fabricated using a process comprising the steps of: (a) forming a floating gate with an overlaying poly oxide layer on a **substrate,** wherein the **floating gate** is etched to have a reentrant angle such that its width generally increases with a distance from the substrate; (b) forming a CVD nitride spacer on the floating gate using a CVD nitride deposition, then anisotropic etching the CVD nitride to form a nitride spacer adjacent to the floating gate; (c) forming a control gate on the floating gate wherein the control gate and the floating gate are sepd. by the poly oxide and the nitride spacer; and (d) forming a **source** and **drain** in the **substrate** using a **source** and **drain** implantation.
IT **7440-21-3,** Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**flash memory** cell using poly to poly tunneling for erase and fabrication using)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L147 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:529202 HCAPLUS
DN 133:113666
TI Fabricating method of nonvolatile **flash memory** device
IN Hong, Gary
PA United Semiconductor Corp., Taiwan
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6096605	A	20000801	US 1998-76676	19980512
PRAI	TW 1997-86119672	A	19971224		

AB A method of fabricating a nonvolatile **flash memory** device, wherein a gate structure is formed on a substrate. The method includes at least the following steps. The substrate is implanted with 1st ions to form a **source** region in the **substrate**. A tunneling oxide layer is formed on the substrate. A Si nitride layer is formed on the substrate. The Si nitride is etched back to form a Si nitride spacer on the sides of the gate structure. The substrate is implanted with 2nd ions to form a **drain** region in the **substrate**. An oxide layer is formed over the **substrate** and the **gate** structure. Then, a polysilicon layer is formed on the oxide layer. The gate structure was used as a selection gate, the Si nitride spacer was used to store electrons, and the polysilicon layer was used as a controlling gate. The **flash memory** device can free memory cells by from the influences of over-erased effect.

IT **7440-38-2D**, Arsenic, ions, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(implantation; in fabricating method of non-volatile **flash memory** device)
RN 7440-38-2 HCAPLUS
CN Arsenic (7CI, 8CI, 9CI) (CA INDEX NAME)

As

IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabricating method of non-volatile **flash memory** device)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O══Si══O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L112 ANSWER 9 OF 25 HCAPLUS

AN 2000:830356 HCAPLUS

DN 133:368478

TI **Floating gate** engineering to improve **tunnel** oxide reliability for **flash memory** devices

IN He, Yue-Song; Chang, Kent K.; Huang, Jiahua

PA Advanced Micro Devices, Inc., USA

SO U.S., 7 pp.
CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6153470	A	20001128	US 1999-374059	19990812

AB A method of forming **floating gate** to improve **tunnel** oxide reliability for **flash memory** devices. A substrate having a **source, drain,** and channel regions is provided. A **tunnel** oxide layer is formed over the substrate. A **floating gate** is formed over the **tunnel** oxide and the channel region, the **floating gate** being multi-layered and having a 2nd layer sandwiched between a 1st layer and a 3rd layer. The 1st layer of the **floating gate** overlying the **tunnel** oxide layer includes an undoped or lightly doped material. The 2nd layer is highly-doped. The 3rd layer is in direct contact with a **dielec.** layer, e.g., an oxide-nitride-oxide **stack,** and is made of an undoped or lightly doped material. A **dielec.** material is formed over the **floating gate** and a **control gate** is formed over the **dielec.** material.

IT **7440-21-3,** Silicon, uses **7631-86-9,** Silica, uses **11105-01-4,** Silicon nitride oxide **12033-89-5,** Silicon nitride, uses **12627-41-7,** Tungsten silicide
RL: DEV (Device component use); USES (Uses)
(in **floating gate** engineering to improve **tunnel** oxide reliability for **flash memory** devices)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS

CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 11105-01-4 HCAPLUS

CN Silicon nitride oxide (9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 12033-89-5 HCAPLUS

CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

L112 ANSWER 4 OF 25 HCAPLUS
AN 2001:221949 HCAPLUS
DN 134:230716
TI Method for forming high density nonvolatile **memories** with high capacitive-coupling ratio
IN Wu, Shye-Lin
PA Texas Instruments-Acer Incorporated, Taiwan
SO U.S., 9 pp., Cont.-in-part of U.S. 6,127,698.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 5

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6207505	B1	20010327	US 1999-326857	19990607
	US 6127698	A	20001003	US 1998-46343	19980323
PRAI	US 1998-46343	A2	19980323		

AB A method for fabricating a high-speed and high-d. nonvolatile **memory** cell is disclosed. First, a semiconductor substrate with defined field oxide and active region is prepd. A **stacked** Si oxide/Si nitride layer is deposited and then the **tunnel** oxide region is defined. A thick thermal oxide is grown on the non-**tunnel** region. After removing the masking Si nitride layer, the **source** and **drain** are formed by an ion implantation and a thermal annealing. The pad oxide film is then removed. A polysilicon film is deposited over the substrate 2 and then oxidized into sacrificial oxide layer. After stripping the sacrificial oxide layer, a rugged topog. is then formed on the doped substrate regions. Thereafter, a thin oxide is grown on the rugged doped substrate region to form a rugged **tunnel** oxide. Finally, the **floating gate**, the interpoly **dielec.**, and the **control gate** are sequentially formed, and the **memory** cell is finished.
IT **7440-21-3**, Silicon, uses **7631-86-9**, Silica, uses **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); USES (Uses)
(method for forming high d. nonvolatile **memories** with high capacitive-coupling ratio)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

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RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***
IT **1314-61-0**, Tantalum oxide (Ta2O5) **37305-87-6**, Barium strontium titanate
RL: DEV (Device component use); TEM (Technical or engineered material

L112 ANSWER 10 OF 25 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:785888 HCAPLUS
DN 133:328511
TI Method for forming **flash memory** of ETOX cell programmed by band-to-band **tunneling** induced substrate hot electron and read by gate induced **drain** leakage current
IN Chi, Min-hwa
PA Taiwan Semiconductor Manufacturing Corp., Taiwan
SO U.S., 12 pp., Cont.-in-part of U.S. Ser. No. 378,197.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6143607	A	20001107	US 1999-411133	19991001
	US 6084262	A	20000704	US 1999-378197	19990819
PRAI	US 1999-378197	A2	19990819		

AB A method of forming an ETOX-cell in a semiconductor substrate is disclosed. The method begins with forming a p-well in the substrate. Then, a **drain** region and a **source** region is formed in the p-well. The **drain** region is of a 1st dopant type and the **source** region is of a 2nd dopant type (i.e. same as the dopant type of the p-well). A **floating-gate** and **tunnel** oxide **stack** is formed above the p-well, the **floating gate** formed between the **drain** region and the **source** region and only after the **drain** region and the **source** region have been formed. The **floating gate** is doped with the same dopant type as the p-well. Finally, a **control gate** is formed above the **floating-gate**, the **floating-gate** and the **control gate** sepd. by a **dielec**. layer. The new ETOX cells can be organized into a NOR array, but with no need of **source** line connections. Each cell is programmed by band-to-band induced substrate hot-electron (BBISHE) at the **source**, and read by GIDL at the **drain** side.

IT **7631-86-9**, Silica, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for forming **flash memory** of EPROM **tunnel** oxide **flash memory** cell programmed by band-to-band **tunneling** induced substrate hot electron and read by gate induced **drain** leakage current)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

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IT **7440-21-3**, Silicon, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; method for forming **flash memory** of EPROM **tunnel** oxide **flash memory** cell programmed by band-to-band **tunneling** induced substrate hot electron and read by gate induced **drain** leakage current)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

L112 ANSWER 22 OF 25 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:175190 HCAPLUS
DN 126:180003
TI Fabricating a fast programming **flash** EEPROM cell
IN Ranaweera, Jeewika Chandanie; Kalastirsky, Ivan; Gulerson, Elvira; Ng, Wai Tung; Salama, Clement Andre T.
PA Ranaweera, Jeewika Chandanie, Can.; Kalastirsky, Ivan; Gulerson, Elvira; Ng, Wai Tung; Salama, Clement Andre T.
SO PCT Int. Appl., 45 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9702605	A1	19970123	WO 1996-CA446	19960703
	CA 2226015	AA	19970123	CA 1996-2226015	19960703
	AU 9661851	A1	19970205	AU 1996-61851	19960703
PRAI	US 1995-1046P	P	19950703		
	WO 1996-CA446	W	19960703		

AB In a **flash** EEPROM cell having **source** and **drain** regions disposed in a substrate, a channel region between the **source** and **drain** regions, a **tunnel dielec.** layer overlying the channel region, a **floating gate** (preferably of polysilicon) overlying the **tunnel dielec.** layer, an interpoly **dielec.** layer overlying the **floating gate**, and a (preferably polysilicon) **control gate** overlying the interpoly **dielec.** layer, the improvement comprises a heavily doped p+ pocket implant covering a portion of the cell width and adjacent to the **source** and/or the **drain** region. The **flash** EEPROM cell is comprised of 2 sections butted together. The portion (widthwise) covered by the heavily doped p+ pocket implant is referred to as the program section and the remaining portion (width-wise) not covered by the p+ pocket implant resembles a conventional EEPROM cell and is referred to as the sense section. The p+ pocket implant and the n+ **drain** and/or **source** regions create a junction having narrow depletion width such that in the event the junction is reverse biased, an elec. field is created for generating hot electrons for storage on the **floating gate**, thereby programming the **flash** EEPROM cell when a high pos. **potential** is **applied** to the **control gate**. The cell according to the present invention provides short programming time and low operating voltages as compared to prior art devices.
IT **7631-86-9**, Silica, processes **12033-89-5**, Silicon nitride (Si3N4), processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabricating a fast programming **flash** EEPROM cell contg.)
RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O=Si=O

RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

L129 ANSWER 8 OF 22 HCAPLUS

AN 2000:785492 HCAPLUS

DN 134:49728

TI Band alignments of high-K dielectrics on Si and Pt

AU Robertson, J.; Riassi, E.; Maria, J-P.; Kingon, A. I.

CS Engineering Dept, Cambridge University, Cambridge, CB2 1PZ, UK

SO Materials Research Society Symposium Proceedings (2000), 592(Structure and Electronic Properties of Ultrathin Dielectric Films on Silicon and Related Structures), 87-92

CODEN: MRSPDH; ISSN: 0272-9172

PB Materials Research Society

DT Journal

LA English

AB Materials with a high **dielec. const.** (K) such as tantalum pentoxide (Ta_2O_5) and barium strontium titanate (BST) are needed for insulators in dynamic random access **memory** capacitors and as gate dielecs. in future silicon devices. The band offsets of these oxides must be over 1 eV for both electrons and holes, to minimize leakage currents due to Schottky emission. The authors have calcd. the band alignments of many high K materials on Si and metals using the method of charge neutrality levels. Ta_2O_5 and BST have rather small conduction band offsets on Si, because the band alignments are quite asym. Other **wide gap** materials Al_2O_3, Y_2O_3, ZrO_2 and $ZrSiO_4$ have offsets of over 1.5 eV for both electrons and holes, suggesting that these are preferable dielecs. Zirconates such as $BaZrO_3$ have wider gaps than the titanates, but they still have rather low conduction band offsets on Si. The implications of the results for future generations of MOSFETs and DRAMS are discussed.

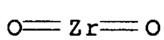
IT **1314-23-4**, Zirconium oxide (ZrO_2), properties **1314-36-9**, Yttrium oxide (Y_2O_3), properties **1314-61-0**, Tantalum oxide (Ta_2O_5) **1344-28-1**, Alumina, properties **7440-06-4**, Platinum, properties **7440-21-3**, Silicon, properties **10101-52-7**, Zirconium silicate ($ZrSiO_4$) **37305-87-6**, Barium strontium titanate

RL: PEP (Physical, engineering or chemical process); PRP (Properties); TEM (Technical or engineered material use); PROC (Process); USES (Uses)

(band alignments of high-**dielec. const.** K **dielecs.** on Si and Pt)

RN 1314-23-4 HCAPLUS

CN Zirconium oxide (ZrO_2) (8CI, 9CI) (CA INDEX NAME)



RN 1314-36-9 HCAPLUS

CN Yttrium oxide (Y_2O_3) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 1314-61-0 HCAPLUS

CN Tantalum oxide (Ta_2O_5) (8CI, 9CI) (CA INDEX NAME)

*** STRUCTURE DIAGRAM IS NOT AVAILABLE ***

RN 1344-28-1 HCAPLUS

CN Aluminum oxide (Al_2O_3) (8CI, 9CI) (CA INDEX NAME)

L129 ANSWER 11 OF 22 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:623320 HCAPLUS
DN 133:342969
TI Barrier layer model determined by XPS data for **tunneling** current reductions at monolayer nitrided Si -SiO2 interfaces
AU Niimi, H.; Yang, H.; Lucovsky, G.; Keister, J. W.; Rowe, J. E.
CS Departments of Materials Science and Engineering, Physics, and Electrical and Computer Engineering, North Carolina State University, Raleigh, NC, 27695-8202, USA
SO Applied Surface Science (2000), 166(1-4), 485-491
CODEN: ASUSEE; ISSN: 0169-4332
PB Elsevier Science B.V.
DT Journal
LA English
AB This paper builds on previous work that has demonstrated that interfacial suboxide transition regions at Si-SiO2 interfaces modify tunneling oscillations in the **Fowler-Nordheim** regime. This paper extends this approach to the direct tunneling regime, emphasizing differences in interfacial transition regions between Si-SiO2 interfaces with and without monolayer level interface nitridation. Tunneling currents in devices with the same oxide-equiv. thickness are reduced by monolayer level interfacial nitrogen with respect to devices without interface nitridation for both substrate and gate injection in both the direct and **Fowler-Nordheim** tunneling regimes. These decreases have been combined with phys. thicker **stacked** oxide/nitride **dielecs**. to yield significantly reduced tunneling compared to devices with oxides of the same equiv. oxide thickness, tox-eq; e.g., tunneling currents .apprx.5.times.10-3 A/cm2 at 1 V for tox-eq.apprx.1.6 nm have been obtained.
IT **7440-21-3**, Silicon, properties **7631-86-9**, Silica, properties **11105-01-4**, Silicon nitride oxide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(barrier layer model detd. by XPS data for tunneling current redns. at monolayer nitrided Si-SiO2 interfaces)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7631-86-9 HCAPLUS
CN Silica (7CI, 8CI, 9CI) (CA INDEX NAME)

O═Si═O

RN 11105-01-4 HCAPLUS
CN Silicon nitride oxide (9CI) (CA INDEX NAME)

L138 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:125740 HCAPLUS
DN 130:161796
TI Method of forming a floating gate in a **flash memory** device
IN Kim, Myung Seon; Back, Sun Haeng
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5872035	A	19990216	US 1997-834398	19970416
	CN 1170959	A	19980121	CN 1997-105579	19970618
PRAI	KR 1996-26485		19960629		

AB The present invention provides a method to maintain a desired width of a floating gate of a **flash memory** device, so that the loss of the capability of storing charges is reduced. The method for forming a floating gate in a **flash memory** device contg. a dielec. layer between said floating gate and a control gate comprises the steps of forming field oxide layers in a semiconductor substrate, forming a gate oxide layer and a cond. layer for said floating gate on said semiconductor substrate, forming a first oxide layer and a silicon nitride layer, in order, on said cond. layer, forming a photoresist pattern, selectively etching said silicon nitride layer, said first oxide layer, and said cond. layer, forming source/drain regions by an ion implantation process, removing said photoresist pattern, forming a passivation layer on the resulting structure and forming a spacer layer on a sidewall of said floating gate by applying an isotropic etching process to said passivation layer so as to prevent said sidewall of said floating gate from being oxidized, forming a **second oxide layer** on said silicon nitride layer, and forming a control gate on the resulting structure.
IT **12033-89-5**, Silicon nitride, uses
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(in forming floating gates in **flash memory** devices)
RN 12033-89-5 HCAPLUS
CN Silicon nitride (Si3N4) (8CI, 9CI) (CA INDEX NAME)